UNIVERSITY OF ENGINEERING AND TECHNOLOGY, TAXILA

FACULTY OF TELECOMMUNICATION AND INFORMATION ENGINEERING

COMPUTER/SOFTWARE ENGINEERING DEPARTMENT

PARALLEL PROCESSING

2K5-CP,SE

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Lecture-5

- Classification of Shared Memory Systems on basis of Interconnection Networks
- Factors for Classification of Interconnection Networks

Classification of Shared Memory Systems on basis of Interconnection Networks

Depending on the interconnection network, a shared memory system leads to systems can be classified as: uniform memory access (UMA), nonuniform memory access (NUMA), and cache-only memory architecture (COMA).

In the UMA system, a shared memory is accessible by all processors through an interconnection network in the same way a single processor accesses its memory. Therefore, all processors have equal access time to any memory location. The interconnection network used in the UMA can be a single bus, multiple buses, a crossbar, or a multiport memory.

In the NUMA system, each processor has part of the shared memory attached. The memory has a single address space. Therefore, any processor could access any memory location directly using its real address. However, the access time to modules depends on the distance to the processor. This results in a nonuniform memory access time. A number of architectures are used to interconnect processors to memory modules in a NUMA.

Similar to the NUMA, each processor has part of the shared memory in the COMA. However, in this case the shared memory consists of cache memory. A COMA system requires that data be migrated to the processor requesting it.

Factors for Classification of Interconnection Networks

Multiprocessors interconnection networks (INs) can be classified based on a number of criteria. These include

(1) mode of operation (synchronous versus asynchronous),
(2) control strategy (centralized versus decentralized),
(3) switching techniques(circuit versus packet)
(4) topology (static versus dynamic).

- Mode of Operation

According to the mode of operation, INs are classified as synchronous versus asynchronous.

In synchronous mode of operation, a single global clock is used by all components in the system such that the whole system is operating in a lock – step manner.

Asynchronous mode of operation, on the other hand, does not require a global clock. Handshaking signals are used instead in order to coordinate

the operation of asynchronous systems. While synchronous systems tend to be slower compared to asynchronous systems, they are race and hazard-free.

- Control Strategy

According to the control strategy, INs can be classified as centralized versus decentralized.

In centralized control systems, a single central control unit is used to over- see and control the operation of the components of the system.

In decentralized control, the control function is distributed among different components in the system. The function and reliability of the central control unit can become the bottle- neck in a centralized control system. While the crossbar is a centralized system, the multistage interconnection networks are decentralized.

- Switching Techniques

Interconnection networks can be classified according to the switching mechanism as circuit versus packet switching networks.

In the circuit switching mechanism, a complete path has to be established prior to the start of communication between a source and a destination. The established path will remain in existence during the whole communication period.

In a packet switching mechanism, communication between a source and destination takes place via messages that are divided into smaller entities, called packets. On their way to the destination, packets can be sent from a node to another in a store-and-forward manner until they reach their destination. While packet switching tends to use the network resources more efficiently compared to circuit switching, it suffers from variable packet delays.

- Topology

An interconnection network topology is a mapping function from the set of pro- cessors and memories onto the same set of processors and memories. In other words, the topology describes how to connect processors and memories to other processors and memories.

A fully connected topology, for example, is a mapping in which each processor is connected to all other processors in the computer.

A ring topology is a mapping that connects processor k to its neighbors.

NEXT LECTURE

- Detailed Study of Interconnection Networks..Part-I