Course Number and Title:	CP-313 Microprocessors and Computer Architecture	
Credit Hours:	3+1	
Pre Requisite	Introduction to Programming, Digital Logic Design	
Instructor:	Dr. M. Irfan Arshad, Engr. Mamoona Khalid	
Lab Engineer:	Engr. Shahwar Ali, Engr. Aleem Zahid	
Compulsory/Elective:	Compulsory	
If Elective: Depth Core/ Breadth Core:		
Course Schedule:	Lecture:	3 hours/week
	Lab:	3 hours/week
	Office hours:	6 hours/week
Course Assessment:	Assignments:	4
	Quizzes:	4
	Course project:	1
	Lab work:	15 Lab. Experiments
	Exams:	Mid-Semester and End-Semester
Grading Policy:	Quizzes:	10%
	Assignments	05%
	Lab work:	15%
	Project:	10%
	Mid-Semester:	20%
	End-Semester:	40%
Text Books:	1. The Intel Microprocessors: 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, Pentium Pro Processor, Pentium II, Pentium III, Pentium 4, Barry B. Brey, Prentice Hall, ISBN: 0131195069, Latest edition. 2. Verilog Digital Systems Design by Zainulabidin Nayabi, McGraw Hill, Latest Edition 3. Advanced Digital Design with Verilog HDL by Ciletti M. D., Latest Edition, Pearson Education.	
Reference Book:	1. Verilog HDL by Painitkar S. Butterworth Heinemann, Latest Edition, Prentice Hall Publisher. 2. Microprocessors: Principles and Application, Charles Gilmore, McGraw Hill, Latest edition. 3. PIC Microcontroller: An Introduction to Software & Hardware Interfacing, Han-Way Huang, Thomson Delmar Learning, ISBN: 1401839673, Latest edition.	
Course Objective:	Hardware description languages (VHDL and Verilog) and synthesis tools are extensively used in industry for quickly designing and implementing complex digital hardware. On completion of this course the students will be able to design and test a blocks of a digital circuit, be able to implement a logic circuits. To acquaint the students with the architecture, programming, interfacing, and applications of microprocessors.	

Course Learning Outcome	CLO Statement	PLO	Bloom
CLO-1:	Differentiate different computer architecture and microprocessor architecture	PLO-2	C4 (Analysis)
CLO-2:	Designing of a microprocessor and its implementation in Assembly.	PLO-3	C5 (Synthesis)
CLO-3:	Programming x86 processor in assembly	PLO-1	C1
Major Topics covered in the course and level of coverage:	Introduction to microprocessors and its Evolution	3 hours	
	8086 family, 8086 internal architecture	3 hours	
	Control unit, internal registers, ALU, Harvard and Van Neumann architectures	6 hours	
	Instruction set Architecture (ISA)	9 hours	
	SRAM, DRAM, Cache Memories, types of Cache	9 hours	
	Hardware and software interrupts, memory-mapped I/O, interrupt-driven and handshake I/O, DMA	9 hours	
	Hardwired State Machine based Design, Micro Program State Machine based Design	3 hours	
	Address mapping using pages	3 hours	
	introduction to parallel processing	3 hours	
Program learning outcomes and how they are covered by specific course outcomes:	**Detailed Contents**	CLO	PLO
	Introduction to microprocessor, basic concepts, control unit, internal registers,	CLO-1	PLO-2
	Designing of Arithmetic and Logic Unit (ALU), Register Transfer Level (RTL), Micro-operations representation through RTL.	CLO-1, 2	PLO-2, 3
	Generation of Control word, Control word representation of micro-operations,	CLO-1, 2	PLO-2, 3
	Register transfer level (RTL) design with Verilog, elements of Verilog, Verilog language concepts, Verilog simulation model, detailed modeling, RT level design and test, HDL coding for synthesis,	CLO-1, 3	PLO-1, 2
	Logic synthesis, reuse methodology, combinational and sequential circuit description, digital design of high speed computational unit, digital design of function generator, digital signal processing algorithm design.	CLO-2	PLO-1, 3
	The instruction set Architecture (ISA's): Three-address ISA's, Two-address ISA's, One-address ISA's, Zero-address ISA's.	CLO-3	PLO-1
	Stack Architecture using push & pop, Reverse Polish Notation (RPN), Data transfer logic operations and branching, programmed I/O interrupts, digital data and display, analogue data input & output, microprocessor system design, assembly language Programming and testing.	CLO-2	PLO-3
	Memory Architecture, RAM, SRAM, DRAM, Cache Designing.	CLO-2	PLO-1, 3
	Microprocessor state, an 8-bit microprocessor	CLO-2	PLO-1, 3

	(8085A or Z-80 or 6800), timing and sequencing, power-on and manual RESET, interfacing, memory and I/O synchronization:		
	The wait state, hardware single stepping, memory speed requirements, logic levels, loading and buffering.	CLO-2	PLO-1, 3
	Microcontroller, single-chip microprocessor, an introduction to microcontrollers,	CLO-2	PLO-3
	8051 Architecture: The 8051 internal RAM and registers, the 8051 interrupts systems, the 8051 instruction set Architecture.	CLO-2	PLO-1, 3
	Microcontrollers on the 8051 family, developing microprocessor-based products,	CLO-1, 3	PLO-1, 2
	Digital system design automation with Verilog, digital design flow, Verilog HDL. Introduction to the design process, preparing the specification,	CLO-2, 3	PLO-1, 3
	Developing a design, implementing and testing the design, design tool for microprocessor development	CLO- 3	PLO-1

Mapping of CLOs with PLOs and Bloom's Taxonomy Cognitive Levels:

PLO	1	2	3	4	5	6	7	8	9	10	11	12
CLO-1		C4										
CLO-2			C5									
CLO-3	C1											

Mapping of CLOs with Assessment Methods:

CLOs/Assessment	CLO-1	CLO-2	CLO-3		
Assignments:	√	√	√		
Quizzes:	√	√	√		
Course project:			√		
Lab work:		√	√		
Mid-Semester:	√	√			
End-Semester:	√	√	√		